Remarks

Applicants respectfully request reconsideration of this application as amended. No claims have been amended. No claims have been cancelled. Therefore, claims 1-32 are presented for examination.

Claims 1-5, 14-16, 19-21, and 30-32 stand rejected under 35 U.S.C. §102(e) as being anticipated by Gulick et al. (U.S. Patent No. 6,532,019). Applicants submit that the present claims are patentable over Gulick.

Gulick discloses a personal computer system that includes a processor module and interface module. The processor module includes a link interface 205 coupled to a link interface 207 in the interface module via a high speed packet based interconnect (link) that connects the processor module and the interface module 203. One set of wires on the link includes data lines connecting a transmit controller 215 in the processor module to a receive controller 216 in the interface module. A second set of wires on link includes data lines connecting a transmit controller 221 in the interface module to a receive controller 222 in the processor module 201. The transmit and receive controllers provide the control logic for link operations. See Gulick at col. 3, ll. 3-22.

Further Gulick discloses that the link includes a link layer, a protocol layer, and a physical layer, and that there is a virtual channel in the link layer for each functional unit connected to the bus. For example, the processor module may include three channels and the interface module 203 may include five virtual channels. Further, it is disclosed that each channel in the link layer includes FIFOs and queues of addressing information and data that have been sent across the link or that will be sent across the link. Thus, an asynchronous transmit FIFO(s) store asynchronous data that will be sent across the bus while an

asynchronous receive FIFO(s) store asynchronous data received from the protocol layer, as well as other FIFOs (col. 4, ll. 21-61).

Claim 1 of the present application recites a queue mechanism divided to include a first functional unit block (FUB) at a first physical partition on a chipset die to perform a first set of functions for the queue mechanism and a second FUB at a second physical partition on the chipset die to perform a second set of functions for the queue mechanism. Applicants submit that nowhere in Gulick is there disclosed a first FUB at a first physical partition on a die to perform a first set of functions for the queue mechanism and a second FUB at a second physical partition on the chipset die to perform a second set of functions for the queue mechanism.

Gulick discloses a link interface having transmit and receive controllers that are explicitly described as being provided to as control logic for link operations. Therefore, the transmit and receive controllers within the link interface cannot be construed as FUBs of a queue mechanism. Gulick also discloses each virtual channel in a link layer includes FIFOs and queues of addressing information and data that have been sent across the link or that will be sent across the link. The Office action maintains that based on such queues "it is inherent that the first FUB and the second FUB are at a first and second physical partition on the chipset die, respectively." See Office Action at page 3, ll. 3-5.

Applicants submit that is not clear how FIFOs/queues associated with virtual channels make it inherent that transmit and receive controllers within the link interface are at first and second physical partitions on a chipset die. First, the link layer in which the FIFOs/queues are associated is a link component, not an interface component. Thus, there is no direct relationship between the link interface and the FIFOs/queues that would make it

inherent that the transmit and receive controllers within the link interface are at first and second physical partitions on a chipset die.

Moreover, it is not inherent that the FIFOs/queues are located at separate physical partitions. The "virtual" channels are associated with the same physical link. Thus, it is likely that the respective FIFOs/queues are located at the same physical location. Nevertheless, there is no disclosure in Gulick of the FIFOs/queues, or any components associated with the FIFOs/queues, being located at separate physical partitions. Consequently, Gulick does not disclose a first FUB at a first physical partition on a die to perform a first set of functions for the queue mechanism and a second FUB at a second physical partition on the chipset die to perform a second set of functions for the queue mechanism. As a result, claim 1 is patentable over Gulick.

Claims 2-13 depend from claim 1 and include additional features. Thus, claims 2-13 are also patentable over Gulick.

Claim 14 recites a queue mechanism divided to include a first functional unit block (FUB) at a first physical partition on an IC die to perform a first set of functions for the queue mechanism and a second FUB at a second physical partition on the IC die to perform a second set of functions for the queue mechanism. Therefore, for the reasons described above with respect to claim 1, claim 14 is also patentable over Gulick. Since claims 15-18 depend from claim 14 and include additional features, claims 15-18 are also patentable over Gulick.

Claim 19 recites a queue mechanism divided to include a first functional unit block (FUB) at a first physical partition on an IC die to perform a first set of functions for the queue mechanism and a second FUB at a second physical partition on the IC die to perform a second set of functions for the queue mechanism. Accordingly, for the reasons described

above with respect to claim 1, claim 19 is also patentable over Gulick. Because claims 20-29 depend from claim 19 and include additional features, claims 20-29 are also patentable over Gulick.

Claim 30 recites a queue mechanism divided to include a first functional unit block (FUB) at a first physical partition on a MCH to perform a first set of functions for the queue mechanism and a second FUB at a second physical partition on the MCH to perform a second set of functions for the queue mechanism. Thus, for the reasons described above with respect to claim 1, claim 30 is also patentable over Gulick. Since claims 31 and 32 depend from claim 30 and include additional features, claims 30 and 32 are also patentable over Gulick.

Claims 6-13, 17-18, and 22-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gulick in view of Cavanna et al. (U.S. Patent No. 6,208,703). Applicants submit that the present claims are patentable over Gulick even in view of Cavanna.

Cavanna discloses a one stage first-in-first-out synchronizer that includes a producer side and a consumer side. The producer side includes a first write buffer, a not full output, a write input, a second write buffer and a write clock input. The first write buffer stores a write pointer. The not full output indicates whether new data may be written. The write input is asserted to write data. The second write buffer receives as input a read pointer. The write clock input is used to provide a clock signal to the first write buffer and the second write buffer. The consumer side includes a first read buffer, a not empty output, a read input, a second read buffer, and a read clock input. The first read buffer stores the read pointer. The not empty output indicates whether stored data may be read. The read input is asserted to read data. The second read buffer receives as input the write pointer. The read clock input is

used to provide a clock signal to the first write buffer and the second write buffer. See Cavanna at Abstract.

Nonetheless, Cavanna does not disclose or suggest a queue mechanism divided to include a first functional unit block (FUB) at a first physical partition on an IC die to perform a first set of functions for the queue mechanism and a second FUB at a second physical partition on the IC die to perform a second set of functions for the queue mechanism. As discussed above, Gulick does not disclose or suggest such a feature. Thus, any combination of Gulick and Cavanna would also not disclose or suggest the feature. Consequently, the present claims are patentable over Gulick in view of Cavanna.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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